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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Application Number: 09/712,873
Filing Date: November 15, 2000
Appellant(s): KRIDNER, JASON D.

Georgios A. Georgakis

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4 January 2006 appealing from the Office action mailed 29 June 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

DeLuca et al US Patent No 5,612,682

Tran US Patent No. 5,734,729

Seo et al US Patent No 5,063,597

Nagata US Patent No. 6,114,981

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-18 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca et al US Patent No 5,612,682 in view of Seo et al US Patent No 5,063,597, Tran US Patent No. 5,734,729, and Nagata US Patent No. 6,114,981. DeLuca discloses method for controlling utilization of a process added to a communications device. Seo teaches a muting circuit in a digital audio system. Nagata teaches a D/A converter.

With regards to claims 1 and 12, DeLuca teaches a digital signal processor (DeLuca, column 4 lines 59-67) operable to provide digital data output (DeLuca, column 7 lines 34-38), determines an authorization state (DeLuca, column 6 lines 41-49), and

generate a disable signal (DeLuca, column 6 lines 49-52). DeLuca fails to teach a digital to analog converter operable to receive the disable signal and the disable signal being generated when a sleep condition is met. Seo teaches a digital to analog converter (Seo, column 3 lines 32-38) coupled to a digital signal processor and operable to receive the digital data output (Seo, Figure 4 Items 41 and 40), convert the digital data to corresponding analog data (Seo, column 3 lines 32-38), output the corresponding analog data (Seo, column 3 lines 32-38, Figure 2C), mute the output of the corresponding analog data (Seo, column 3 lines 32-38), receive the disable signal (Seo, column 3 lines 32-34), and mute the output of the corresponding analog data in response to the disable signal (Seo, Figures 2B and 2C, column 3 lines 14-38). Nagata teaches a digital to analog converter including an input operable to receive the disable signal (Nagata, column 4 lines 28-49, D/A converter with mute control, Figure 3, column 1 lines 51-61). Tran teaches a disable signal generated when the electronic device satisfies one or more sleep conditions (Tran, column 2 lines 34-42). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize Seo's method of muting in response to a disable signal, Tran's method of disabling when a sleep condition is met, and Nagata's placement of the disable signal with DeLuca's communication device because it offers the advantage of providing an improved muting system that limits disturbing noises that are generated during the process of turning off power to the system or by external influences (Nagata, column 1 lines 35-50) and the reduction of transient noises associated with shutdowns or sleep modes (Tran, column 2 lines 34-42).

With regards to claims 2, 10 and 15, DeLuca as modified teaches the authorization state either being positive or negative (DeLuca, column 6 lines 42-52) and further teaches the digital signal processor operative to generate the disable signal when the authorization state is negative (DeLuca, column 7 lines 2-7).

With regards to claim 3, Deluca as modified teaches the serial input for receiving timing signals to enable reception of the disable signal (Seo, column 3 lines 55-58).

With regards to claims 4 and 13, DeLuca as modified teaches the output muted by filtering the received digital data prior to conversion into analog data (Seo, column 3 lines 3-31).

With regards to claim 5, DeLuca as modified teaches the output pin operable to transmit the disable signal as a high voltage (Seo, column 3 lines 50-51).

With regards to claim 6 (as best understood), DeLuca as modified teaches the output pin operable to transmit a low voltage in the absence of a disable signal (Seo, column 3 lines 50-54).

With regards to claims 7 and 11, DeLuca as modified teaches the authorization state is either positive or negative and the DSP is not operable to generate the disable signal when the authorization state is negative (DeLuca, column 10 lines 15-24).

With regards to claims 8 and 16-17, DeLuca as modified teaches the digital signal processor having at least two output pins where the first pin provides a clock signal and the second pin provides a disable signal and the state of the disable signal at the rising edges of the clock signal re read by the converter (Seo, column 2 lines 62-66, column 3 lines 14-18).

With regards to claims 9 and 14, DeLuca as modified teaches an analog amplifier operable to receive the disable signal after analog conversion (Seo, Figure 1).

With regards to claim 18, DeLuca as modified teaches the generating of a power-save signal (Seo, column 3 lines 42-44) where the disable signal is generated in response to the power-save signal (Seo, column 3 lines 50-54).

With regards to claim 21, DeLuca as modified teaches one of the sleep conditions is usage of the electronic device (DeLuca, column 7 lines 30-52).

With regards to claim 22, DeLuca as modified teaches the electronic device being a music player, video player, or multimedia file player (DeLuca, column 5 lines 8-22).

Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca et al US Patent No 5,612,682, Seo et al US Patent No 5,063,597, Tran US Patent No. 5,734,729, and Nagata US Patent No. 6,114,981 as applied to claim 12 above, and further in view of Lipovski US Patent No 6,675,002.

With regards to claims 19-20, DeLuca as modified fails to teach the generating of an override signal in response to a disable signal. Lipovski teaches the generating of an override signal in response to the step of generating a disable signal and terminating the muting step in response to the override signal (Lipovski, column 6 lines 33-44). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize Lipovski's method of overriding a disable signal because it offers

the advantage of allowing sound output in the event of an emergency (Lipovski, column 6 lines 33-36).

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca et al US Patent No 5,612,682, Seo et al US Patent No 5,063,597, Tran US Patent No. 5,734,729, and Nagata US Patent No. 6,114,981 as applied to claim 12 above, and further in view of Elliot US PGPub 2002/0077177.

With regards to claim 23, DeLuca as modified teaches selecting a data file (Tran, column 5 lines 8-22), but fails to teach performing a hash function on the data file by the DSP. Elliot teaches performing a hashing function on the data to generate the mathematical function result wherein the hashing function is executed by the digital signal processor (Elliot, pages 16-17, paragraph 0192). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize Elliot's hashing method with DeLuca as modified because it offers the advantage of providing assurances that files are uncorrupted (Elliot, pages 16-17, paragraph 0192).

(10) Response to Argument

In the instant appeal brief, Applicant has argued that the Examiner has failed to make a prima facie case of obviousness when combining the Deluca, Seo, Tran, and Nagata references. Specifically, Applicant has argued that:

I. The Seo reference teaches away from the present invention by teaching a first switching circuit that receives a mute signal and not the digital to analog converter receiving the mute signal (Appeal Brief, page 6).

II. The Seo reference fails to teach the digital to analog converter receiving a disable signal (Appeal Brief, page 6).

III. The combination has no reasonable expectation of success because of the absence of teachings for all the claim limitations and because the Seo reference teaches away from the present invention (Appeal Brief, page 7).

Examiner respectfully disagrees with these assertions.

I. The Seo reference does not teach away from the present invention.

Applicant has argued that the Seo reference teaches away from the present invention because the Seo reference teaches a first switching circuit receiving a disable signal instead of the digital to analog converter receiving the disable signal as presented in claim 1. Examiner respectfully disagrees. The Seo reference does not teach away from the present invention. Seo teaches a first switching circuit that receives a mute control signal (Seo, column 3 lines 32-38). The switching circuit selectively outputs data to the digital to analog converter in response to this mute signal (Seo, column 3 lines 32-38) and the digital to analog converter then outputs either a muted signal or a non-muted signal based upon the input from the switching circuit (Seo, column 3 lines 32-

38). This teaching does not support a claim that the Seo reference teaches away from the present invention.

In Syntex LLC v. Apotex, Inc., 04-1252 (Fed. Cir. May 18, 2005) (Gajarsa, J.) the court noted that "a prior art reference that does not specifically refer to one element of a combination **does not**, per se, teach away" (see Syntex v Apotex, page 15). The court further noted "a statement that a particular combination is not a preferred embodiment does not teach away **absent clear discouragement** of that combination" (see Syntext v Apotex, page 15). Hence, a reference does not teach away from an invention merely because it does not specifically teach one element and clear discouragement of a combination is required in order to support a claim that a reference teaches away.

The Seo reference in no way provides any discouragement against a modification where the disable signal would directly input into the digital to analog converter. The Seo reference does not specifically teach the digital to analog converter receiving the disable signal; however, just as in Syntex, the mere fact that the feature is not disclosed does not support a finding that the reference teaches away. Applicant has asserted that Seo specifically teaches not to output the disable or mute signal to a digital to analog converter (Appeal Brief, page 6); however, this assertion is unfounded. Applicant has not cited any portion of the Seo reference that shows a clear statement against the inputting of a mute or disable signal into a digital to analog converter. Seo in no way teaches not to output the disable or mute signal to a digital to analog converter. Instead Seo merely teaches an alternative arrangement. Thus, the Seo reference does not teach away from the present invention.

II. Applicant's argument that the Seo reference fails to teach the digital to analog converter receiving a disable or mute signal is unfounded because Examiner has relied upon the Nagata reference for this feature.

Applicant has argued on pages 6-7 that the Seo reference fails to teach "a digital to analog converter ... operable to ... mute the output of the corresponding analog data." This argument is unfounded because in the rejection of claim 1 Examiner has relied upon the Nagata reference to teach this feature (see Final Rejection mailed 6/29/2005, rejection of claim 1, page 3). Examiner noted in the final rejection that the primary reference, Deluca, fails to teach a digital to analog converter receiving a disable signal. Examiner then asserted that Nagata teaches a digital to analog converter receiving a disable signal (Nagata, column 4 lines 28-49, D/A converter with mute control, Figure 3, column 1 lines 51-61) and noted that the modification would provide the benefit of an improved muting system that limits disturbing noises that are generated during the process of turning off power to the system or by external influences (Nagata, column 1 lines 35-50). The Nagata reference is directed towards an over-sampling digital to analog converter that has a mute function (Nagata, Abstract). Examiner intended the Nagata reference to show only this feature of a digital to analog converter with a mute signal input. Applicant has not disputed that the Nagata reference teaches this feature nor has Applicant disputed that the Nagata reference provides ample motivation to combine. Instead, Applicant has asserted that Seo fails to

teach the limitation. Examiner relied upon the Seo reference to show the interoperating of a digital to analog converter and a digital signal processor as is provided in claim 1 (see Final Rejection mailed 6/29/2005, rejection of claim 1, page 3). As noted above, the primary reference Deluca and the Seo reference are silent as to a digital to analog converter including a mute or disable signal. Hence, the Nagata reference was included in order to remedy the deficiency in the primary reference, Deluca. As a result, Applicant's argument against the Seo reference failing to teach a digital to analog converter receiving a disable or mute signal is without merit because the Examiner did not rely upon Seo to teach this feature.

III. The combination of DeLuca, Tran, Seo, and Nagata has a reasonable expectation for success.

Applicant has argued that there is no reasonable expectation for success in combining the DeLuca, Tran, Seo, and Nagata references. Applicant bases this argument on the allegation that the references fail to teach all of the recited claim limitations and the allegation that the Seo reference teaches away. Examiner respectfully disagrees with this assertion.

As noted above, Applicant's assertion that the references fail to teach all of the recited claim limitations is without merit. Applicant has focused upon the alleged lack of teaching of a digital to analog converter receiving a disable or mute signal and has asserted that Seo's lack of teaching of this feature undermines the Examiner's prima

facae case. This assertion fails because Examiner has relied upon the Nagata reference to teach this feature. Applicant has not disputed that the Nagata reference teaches this feature. Thus, the combination of DeLuca, Tran, Seo, and Nagata teach all of the claimed limitations.

Futher, Applicant's argument against the reasonable expectation for success fails because the Seo reference does not teach away from the present invention. As noted above, the Seo reference does not provide any discouragement against the modification to a digital to analog converter whereby a disable or mute signal would be received by the digital to analog converter. As a result, Examiner's use of the Nagata reference to teach this feature is proper.

Applicant's two bases for asserting that the combination of DeLuca, Tran, Seo, and Nagata both fail and as a result the combination of the cited references is proper.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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